x86 Instruction Set Architecture

Tom Shanley

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The **Instruction Set Architecture**, or ISA, is defined as that part of the processor architecture related to programming, including the native data types, instructions, registers, addressing modes, memory architecture, interrupt and exception handling, and external IO. With the exception of some small deviations and differences in terminology, all Intel and AMD x86 processors share a common ISA. This book focuses on those shared attributes (it does not cover those areas where the two companies have chosen widely divergent solutions which, by definition, fall outside of the ISA specification). If you re looking for a comprehensive book designed to bootstrap you up quickly on virtually all aspects of the x86 32/64-bit Instruction Set Architecture (ISA), we respectfully ask you to consider this book.

Essential topics covered include:

- Basic Terms and Concepts
- Operating Mode/SubMode Introduction
- A (very) Brief History
- State After Reset
- Intro to the IA-32 Ecosystem
- Instruction Set Expansion
- 32-bit Machine Language Instruction Format
- Real Mode (8086 Emulation)
- Legacy x87 FP Support
- Introduction to Multitasking
- Multitasking-Related Issues
- Summary of the Protection Mechanisms
- Protected Mode Memory Addressing
- Code, Calls and Privilege Checks
- Data and Stack Segments
- IA-32 Address Translation Mechanisms
- Memory Type Configuration
- Task Switching
- Protected Mode Interrupts and Exceptions
- Virtual 8086 Mode
- The MMX Facilities
- The SSE Facilities
- IA-32e OS Environment
- IA-32e Address Translation
- Compatibility Mode
- 64-bit Register Overview
- 64-bit Operands and Addressing
- 64-bit Machine Language Instruction Format
- 64-bit Odds and Ends
- Transitioning to Protected Mode
- Transitioning to IA-32e Mode
- Introduction to Virtualization Technology

- System Management Mode (SMM)
- Machine Check Architecture (MCA)
- The Local and IO APICs

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Richard Vazquez:

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